

METHOD FOR MANUFACTURING A WAFER LEVEL CHIP SCALE PACKAGE

The present application claims priority from Korean Patent Application No. 2002-64513 filed October 22, 2002, the contents of which are incorporated herein by reference in
5 their entirety.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a method for manufacturing a wafer level chip scale
10 package.

2. Description of the Related Art

Lately, the electronic industry has been seeking to manufacture electronic products that are extremely small, light weight, operate at high speeds, have multiple functions and
15 have high performance, all at an effective cost. One of the methods used to try to attain such a goal is a package assembly technique. Thanks to this technique, new types of packages have been developed, for example, a chip scale or chip size package (CSP). The CSP has a number of advantages over typical plastic packages. Of all the advantages, the most important is the package size. According to international semiconductor associations, such as the Joint
20 Electron Device Engineering Council (JEDEC), and Electronic Industry Association of Japan (EIAJ), the CSP is defined as a package whose size is not larger than 1.2 times the size of the chip.

The CSP has been mainly employed in electronic products requiring miniaturization and mobility, such as digital camcorders, portable telephones, notebooks, and memory cards.
25 CSPs include semiconductor devices such as digital signal processors (DSP), application specific integrated circuits (ASIC), and micro controllers. CSPs also include memory devices such as dynamic random access memories (DRAM) and flash memories. Use of CSPs having memory devices is steadily increasing. Over fifty varieties of CSPs are at present being developed or produced all over the world.

30 The CSP has, however, some drawbacks. For example, there are some difficulties in obtaining acceptable reliability of the package. Further, the CSP needs additional equipment requiring large quantities of raw and/or subsidiary materials and high per unit costs of production, which causes a reduction in price competition.

In order to overcome these drawbacks, a wafer level chip scale package (WLCSP) has appeared as a solution.

Generally, a package is manufactured through wafer fabrication, cutting, and assembly processes. The package assembly process employs separate equipment and raw/subsidiary materials from those of the wafer fabrication process. The WLCSP, however, can allow manufacture of the packages as final products at wafer level, i.e. without dividing them into individual chips. The WLCSP can apply the equipment and processes used for the wafer fabrication process to complete the package assembly process as well. Therefore, the WLCSP may allow the manufacture of packages at a more effective cost.

FIG. 1 is a plan view of a conventional WLCSP 20. FIG. 2 is a cross-sectional view taken along the line 2-2 in FIG. 1. Solder balls (28 of FIG. 2) are not illustrated in FIG. 1 to illustrate a ball pad 23.

Referring to FIGS. 1 and 2, a CSP 20 comprises a semiconductor chip 14. The semiconductor chip 14 has a plurality of chip pads 11. The chip pads 11 are disposed at the periphery of an upper surface of a silicon substrate 12. A metal wiring layer 21 is formed for redistribution of the chip pad 11. The solder balls 28 are formed on ball pads 23 located at the ends of the metal wiring layer 21.

The semiconductor chip 14 comprises the chip pads 11 and a passivation layer 13. The chip pads 11 are electrically connected to an integrated circuit (IC) of the silicon substrate 12. The passivation layer 13 protects the IC and the chip pads 11. The chip pads 11 are made of Al and the passivation layer 13 is made of oxide film or nitride film.

A dielectric layer 22 (hereinafter referred to as a first dielectric layer) is formed on the passivation layer 13 at a predetermined thickness, and is used for formation of the metal wiring layer 21. The first dielectric layer 22 overlies the passivation layer 13, leaving a portion of each chip pad 11 exposed.

A metal base layer 25 is formed on the chip pad 11 and the first dielectric layer 22, in the position on which the metal wiring layer 21 is to be formed.

The metal wiring layer 21 is formed on the first dielectric layer 22 toward the center of the silicon substrate 12. The metal wiring layer 21 is connected to the chip pads 11. The ball pads 23 are formed at the ends of the metal wiring layer 21 for formation of the solder balls 28.

Another dielectric layer 24 (hereinafter referred to as a second dielectric layer) is formed to a predetermined thickness on the entire surface of the silicon substrate 12 except

for the ball pads 23. The second dielectric layer 24 covers the passivation layer 13, the metal wiring layer 21, and the first dielectric layer 22.

After the solder ball 28 is placed on a ball pad 23, the solder ball 28 is fixed or connected to the ball pad 23 through a solder reflow process using heat.

5 The conventional CSP 20 has several disadvantages. For example, the size of the solder ball 28 is small and the ball pad 23 is exposed only through a connection hole 27 formed in the second dielectric layer 24. Thus, the contact area between the ball pad 23 and the solder ball 28 is relatively small. The narrower the pitch between two adjacent ball pads 23 is, the smaller the contact area between the ball pad 23 and the solder ball 28 must be.
10 Therefore, the connection reliability of the solder ball 28 to the ball pad 23 is reduced together with the reduction of the pitch between the ball pads 23. In addition, the ball pad 23 is formed in a circular shape and is enclosed by the second dielectric layer 24. Thus, even though the solder ball 28 is not metallically connected with the second dielectric layer 24, it is in contact with it. This plus the fact that the connection of the solder ball 28 is made only to
15 the flat surface of the ball pad 23 may reduce the connection reliability of the solder ball 28 to the ball pad 23.

SUMMARY OF THE INVENTION

20 An integrated circuit (IC) is created on or in a semiconductor substrate such as silicon substrate by a wafer fabrication process. The IC is electrically connected to a plurality of chip pads. A passivation layer is formed on an upper surface of the substrate for protection of the chip pads and the IC. A semiconductor chip contains both the IC and the chip pads. A semiconductor wafer includes these semiconductor chips and scribe lines. The scribe lines are used to divide the semiconductor chips. A first dielectric layer is formed on the passivation
25 layer, leaving a portion of each chip pad exposed. A second dielectric layer is formed on the first dielectric layer to expose the chip pad. The second dielectric layer has an embossed portion such that a portion of the first dielectric layer where a ball pad is to be formed is exposed. A metal wiring layer is formed on the second dielectric layer and the embossed portion for the redistribution of the chip pad. The metal wiring layer is also connected to the
30 chip pad. A third dielectric layer is then formed on the metal wiring layer and the second dielectric layer for protection of the metal wiring layer. A ball pad is formed by removing a portion of the third dielectric layer located on the embossed portion. A solder ball is placed on the ball pad including the embossed portion of the second dielectric layer. The semiconductor wafer is cut along the scribe lines to obtain wafer level chip scale packages.

The embossed portion may be formed such that the ring shape of the second dielectric layer remains on the exposed circular shape of the first dielectric layer. The embossed portion may include a concave portion of the first dielectric layer and a convex portion of the second dielectric layer. The convex portion may have a discontinuous ring shape. The diameter of the convex portion may be smaller than that of the concave portion. The area of the convex portion may be approximately equal to that of the concave portion inside the convex portion. The first dielectric layer may be formed such that the passivation layer inside the ring-shaped second dielectric layer is exposed.

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BRIEF DESCRIPTION OF THE DRAWINGS

These and other objects, features and advantages of the present invention will be readily understood with reference to the following detailed description thereof provided in conjunction with the accompanying drawings, wherein like reference numerals designate like structural elements, and, in which:

FIG. 1 is a plan view of a conventional wafer level chip scale package;

FIG. 2 is a cross-sectional view taken along the line 2-2 in FIG. 1;

FIGS. 3 through 14 are views illustrating each step of a method for manufacturing a wafer level chip scale package in accordance with an embodiment of the present invention;

FIG. 3 is a simplified plan view of a semiconductor wafer;

FIG. 4 is an enlarged plan view of a portion of a semiconductor device;

FIG. 5 is an enlarged cross-sectional view of the same portion of semiconductor device;

FIG. 6 is a cross-sectional view illustrating the coating of a first dielectric layer;

FIG. 7 is a cross-sectional view illustrating the patterning of the first dielectric layer to expose a chip pad;

FIG. 8 is a plan view illustrating the patterning of a second dielectric layer to expose the chip pad and to form an embossed portion corresponding to a ball pad to be formed later;

FIG. 9 is a cross-sectional view taken along the line 9-9 in FIG. 8, illustrating the patterning of the second dielectric layer to expose the chip pad and to form the embossed portion corresponding to a ball pad to be formed later;

FIG. 10 is a cross-sectional view illustrating the formation of a metal wiring layer to connect the chip pad to the embossed portion;

FIG. 11 is a cross-sectional view illustrating the coating of a third dielectric layer;

FIG. 12 is a plan view illustrating the patterning of the third dielectric layer to expose the embossed portion and consequently to form the ball pad;

FIG. 13 is a cross-sectional view taken along the line 13-13 in FIG. 12, illustrating the patterning of the third dielectric layer to expose the embossed portion and consequently to form the ball pad;

FIG. 14 is a cross-sectional view illustrating a solder ball formed on the ball pad;

FIG. 15 is a plan view of a method for manufacturing a wafer level chip scale package in accordance with another embodiment of the present invention, illustrating another example of the embossed portion;

FIGS. 16 through 21 are views illustrating each step of a method for manufacturing a wafer level chip scale package in accordance with yet another embodiment of the present invention;

FIG. 16 is a cross-sectional view illustrating the patterning of a first dielectric layer to expose a chip pad and to form a first concave portion at the center of an area to be formed as a ball pad;

FIG. 17 is a plan view illustrating the patterning of a second dielectric layer to expose the chip pad and the first concave portion and to form a second concave portion outside the first concave portion;

FIG. 18 is a cross-sectional view taken along the line 18-18 in FIG. 17, illustrating the patterning of the second dielectric layer to expose the first concave portion and to form the second concave portion outside the first concave portion;

FIG. 19 is a plan view illustrating the patterning of a third dielectric layer to expose the embossed portion including the first and second concave portions and consequently to form the ball pad;

FIG. 20 is a cross-sectional view taken along the line 20-20 in FIG. 19, illustrating the patterning of the third dielectric layer to expose the embossed portion including the first and second concave portions and consequently to form the ball pad; and

FIG. 21 is a cross-sectional view of the solder ball formed on the ball pad.

DETAILED DESCRIPTION OF THE INVENTION

Embodiments of the present invention will be described below with reference to the accompanying drawings.

FIGS. 3 through 14 are views illustrating a method for manufacturing a wafer level chip scale package 70 in accordance with an embodiment of the present invention. FIG. 3 is a simplified plan view of a semiconductor wafer 30.

Referring to FIG. 3, an integrated circuit (IC) (not illustrated for simplicity) is formed on a semiconductor substrate such as a silicon substrate 32 using a wafer fabrication process. A wafer 30 has a plurality of semiconductor chips 34 and scribe lines 36 therebetween. The semiconductor chips 34 are divided along the scribe lines 36.

FIG. 4 illustrates schematically a semiconductor chip 34. FIGS. 5 through 14 illustrate a portion of the semiconductor chip 34.

Referring to FIGS. 4 and 5, the semiconductor chip 34 comprises a plurality of chip pads 31 formed on an upper surface of the silicon substrate 32. The chip pads 31 are electrically connected to the IC. A passivation layer 33 covers the upper surface of the silicon substrate 32 and surrounds the chip pads 31 to protect the IC protected from external environments. The chip pads 31 are made of Al and the passivation layer 33 is made of oxide or nitride. Although the chip pads 31 are disposed along the periphery of the semiconductor chip 34 as shown in FIG. 4, the position of the chip pads 31 may not be limited to the periphery of the semiconductor chip 34. For example, the chip pads 32 may be formed on a central portion of the semiconductor chip 34.

Referring to FIGS. 6 and 7, a first dielectric layer 42 is formed on the passivation layer 33. The first dielectric layer 42 serves as a lower dielectric layer for formation of a metal wiring layer on the passivation layer 33. The first dielectric layer 42 is formed to a predetermined thickness on the passivation layer 33, leaving a portion of the chip pads 31 exposed. The first dielectric layer 42 may be made of organic materials which are stress-absorbing, such as polyimide or benzo cyclo butene (BCB). The chip pads 31, as shown in Fig. 7, are exposed through the first dielectric layer 42 using conventional photolithography and etching techniques.

Referring to FIGS. 8 and 9, a second dielectric layer 44 is formed on the first dielectric layer 42 to a predetermined thickness, leaving a portion of the chip pads 31 exposed. The second dielectric layer 44 is patterned such that a portion of the first dielectric layer 42 where a ball pad is to be formed (a ball pad area) is exposed. At this time, the second dielectric layer 44 located within the ball pad area is not completely removed. Rather, a portion of the second dielectric layer 44 remains within the ball pad area, for improved connection reliability between the solder ball and the ball pad. The exposed portion of the first dielectric layer 42 is hereinafter referred to as a concave portion 52. The second

dielectric layer 44 remaining on the ball pad area is hereinafter referred to as a convex portion 54. An embossed portion 50 comprises the concave portion 52 and the convex portion 54. If the ball pad is to be circular, the concave portion 52 is circular and the convex portion 54 is ring-shaped. The embossed portion 50 may increase the contact area with the metal wiring layer, thus improving the connection reliability between the solder ball and the ball pad.

Conventional photolithography and etching techniques are used to expose the chip pads 31 through the second dielectric layer 44 and to embossed portion 50. The second dielectric layer 44 may also be made of a material including, but not limited to, polyimide or BCB.

Referring to FIG. 10, the metal wiring layer 41 is formed for redistribution of each chip pad 31. The metal wiring layer 41 is formed on the chip pad 31, the second dielectric layer 44, and the embossed portion 50 to connect the chip pad 31 to the embossed portion 50. The metal wiring layer 41 may be formed by conventional techniques such as sputtering or chemical vapor deposition methods. The metal wiring layer 41 may be a single layer of Cu or Al, or multi-layered structure of several metals.

Before the formation of the metal wiring layer 41, a metal base layer 45 may be formed where the metal wiring layer 41 is to be formed. The metal base layer 45 may serve as an adhesive, a diffusion barrier, or a plating base layer for the metal wiring layer 41. The metal base layer 45 may be Ti/Cu, Ti/Ti-Cu/Cu, Cr/Cr-Cu/Cu, TiW/Cu, Al/Ni/Cu, or Al/NiV/Cu.

Referring to FIG. 11, a third dielectric layer 46 is formed to a predetermined thickness on the resulting structure. The third dielectric layer 46 covers the passivation layer 33, the metal wiring layer 41, the first dielectric layer 42, and the second dielectric layer 44. The third dielectric layer 46 protects the semiconductor chip 34 by absorbing shocks that may be applied thereto. The third dielectric layer 46 also may serve as a wiring substrate. The third dielectric layer 46 may be made of, for example, polyimide or BCB.

Referring to FIGS. 12 and 13, a portion of the third dielectric layer 46 located on the embossed portion 50 is removed to form a connection hole 47 that expose a ball pad 43. Because the ball pad 43 is electrically connected (redistributed) to the chip pad 31 through the metal wiring layer 41, the exact positions of the ball pad 43 and the chip pad 31 may not be limited.

The area of the convex portion 54 may be approximately equal to the area of the concave portion 52 inside the convex portion 54, for improved connection reliability between the solder ball 60 and the ball pad 43.

Referring to FIG. 14, a solder ball 60 is formed on the ball pad 43. The ball pad 43 is coated with flux. The solder ball 60 is placed on the ball pad 43 and is reflowed. The solder ball 60 is thus electrically connected to the metal wiring layer 41 and the chip pad 31 through the ball pad 43. Because the ball pad 43 contacts the solder ball 60 with the embossed
5 portion, i.e., an uneven contact surface, the contact area between the solder ball 60 and the ball pad 43 may increase, thereby improving the connection reliability between the solder ball 60 and the ball pad 43.

Although the present invention described above employs the ball placement method, the solder ball 60 may be formed by other methods such as plating, stencil printing, or metal
10 jet methods.

After the package is manufactured at wafer level as described above, the packages are divided along the scribe lines (36 of FIG. 3) to obtain the wafer level chip scale package 70.

Although the previously described embodiment shows the convex portion 54 as a continuous ring-shape, the convex portion 54 may have a discontinuous ring-shape, as shown
15 in FIG. 15.

FIGS. 16 through 21 are views illustrating a method for manufacturing a wafer level chip scale package 270 in accordance with another embodiment of the present invention.

Referring to FIG. 16, a first dielectric layer 242 is formed on a passivation layer 233. The first dielectric layer 242 serves as a lower dielectric layer for formation of a metal wiring
20 layer on the passivation layer 233. The first dielectric layer 242 is formed to a predetermined thickness on the passivation layer 233, leaving the chip pads 231 exposed. The first dielectric layer 242 has a first concave portion 252a such that a portion of the passivation layer 233 where a ball pad is to be formed (a ball pad area) is exposed. The first concave portion 252a may be smaller in size than the ball pad to be formed later and may be formed corresponding
25 to the center of the ball pad.

Referring to FIGS. 17 and 18, a second dielectric layer 244 is formed on the first dielectric layer 242 to a predetermined thickness, leaving chip pads 231 exposed. The second dielectric layer 244 is patterned such that a portion of the first dielectric layer 242, where a ball pad is to be formed (the ball pad area), is exposed. At this time, the second dielectric
30 layer 244 located within the ball pad area is not completely removed. Rather, a portion of the second dielectric layer 244 (a convex portion 254) remains within the ball pad area, for improved connection reliability between the solder ball and the ball pad. The exposed portion of the passivation layer 233 inside the convex portion 254 is a first concave portion 252a. The exposed portion of the first dielectric layer 242 outside the convex portion 254 is a

second concave portion 252b. The embossed portion 250 comprises the first and second concave portions 252a and 252b and the convex portion 254. If the ball pad is to be circular, the first and second concave portions 252a and 252b are circular and the convex portion 254 is ring-shaped. The embossed portion 250 may increase the contact area with the metal wiring layer and improve the connection reliability between the solder ball and the ball pad.

Because the formation of the metal wiring layer 241 and the metal base layer 245 in this embodiment are the same as that of the first embodiment, the description thereof is herein omitted.

Referring to FIGS. 19 and 20, a third dielectric layer 246 is formed on the resulting structure to a predetermined thickness. The third dielectric layer 246 located on the embossed portion 250 is removed to form a connection hole 247 that exposes a ball pad 243 and the metal wiring layer 241.

Although this embodiment shows a continuous ring-shaped convex portion 254 between the first concave portion 252a and the second concave portion 252b, the convex portion 254 may be discontinuously formed as shown in FIG. 15.

Referring to FIG. 21, a solder ball 260 is formed on the ball pad 243.

After the package manufacture is completed through the above described embodiments, the wafer is divided along the scribe lines to obtain a wafer level chip scale package 270.

In the embodiment described in FIG.12, only the first dielectric layer 42 is exposed through the concave portions 52 of the embossed portion 50. However, in the embodiment described right above, both the passivation layer 233 and the first dielectric layer 242 are exposed through the first concave portion 252a and second concave portion 252b, respectively.

The ball pad may be selected according to the thicknesses and material properties of the first and second dielectric layers 242, 244. For example, if the second dielectric layer 244 has a thickness of 15 μ m or greater, the ball pad of the embodiment right above (FIG. 18) is preferable. If the second dielectric layer has a thickness of less than 15 μ m, the ball pad shown in FIG. 11 is preferred.

In accordance with the present invention, an embossed portion is formed inside the ball pad and the metal wiring layer is formed on the embossed portion. Thus, the contact area between the solder ball and the metal wiring layer can be significantly increased, thereby improving the connection reliability between the ball pad and the solder ball.

Although the exemplary embodiments of the present invention have been described in detail hereinabove, it should be understood that many variations and/or modifications of the basic inventive concepts herein taught, which may appear to those skilled in the art, will still fall within the spirit and scope of the present invention as defined in the appended claims.